FIG. 1

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
COHERENT MEMORY IN A DISTRIBUTED MEMORY, CACHE COHERENT, MULTI-PROCESSOR SYSTEM"
by Manoj Khare, Akhilesh Kumar, Lily P. Looi
Docket No. P9301   Contact: Cynthia Thomas Faatz   Reg. No. 39,973   Phone No. 53-268-1442
Sheet 2 of 5
REPLACEMENT SHEET

FIG. 2

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
COHERENT MEMORY IN A DISTRIBUTED MEMORY, CACHE COHERENT, MULTI-PROCESSOR SYSTEM"
by Manoj Khare, Akhilesh Kumar, Lily P. Looi
Docket No. P9301   Contact: Cynthia Thomas Faatz   Reg. No. 39,973   Phone No. 53-268-1442
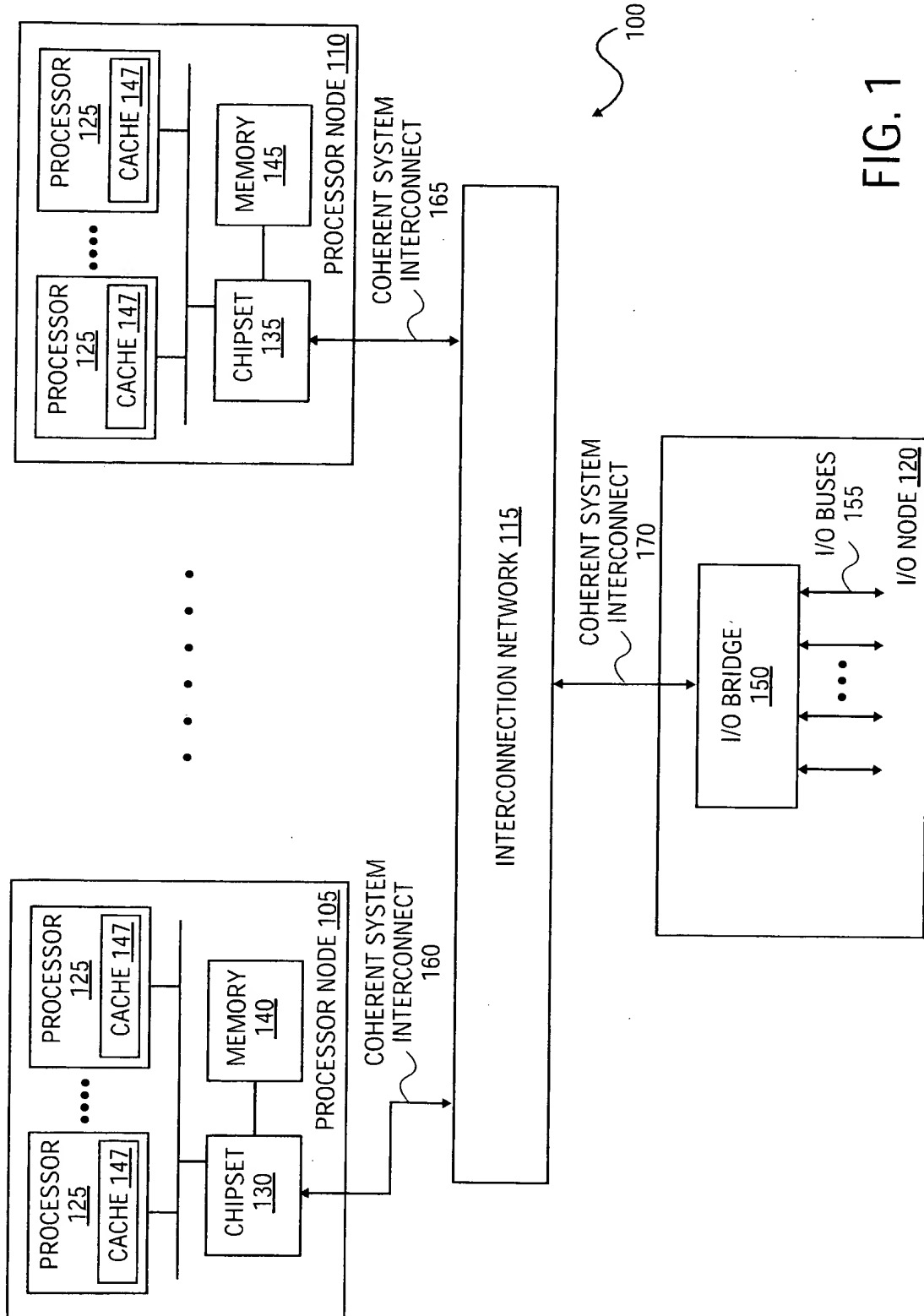Sheet 3 of 5
REPLACEMENT SHEET

FIG. 3

```
                          ┌─────────┐
                          │  BEGIN  │
                          └─────────┘
                               │
                               ▼
              ┌───────────────────────────────────┐
              │ SELECT NEXT ORDERED TRANSACTION    │   405
              │ REQUEST TO RETIRE FROM I/O         │
              │ TRANSACTION REQUEST BUFFER         │
              └───────────────────────────────────┘
                               │
                               ▼
            ◇ READ                          ◇ I/O
            TRANS. OR    WRITE              CACHE BUFFERS    Y
            WRITE TRANS.? ─────────────▶    OWN LINE IN  ──────┐
               415                          EXCLUSIVE STATE?   │
                │ READ                        445              │
                ▼                              │ N            │
            ◇ LINE                             ▼              │
            PRESENT IN I/O   Y          ┌─────────────────┐   │
            CACHE IN VALID ────┐        │ ACQUIRE OWNERSHIP│ 455│
            STATE?             │        │ OF LINE          │   │
              420             │        └─────────────────┘    │
               │ N           │                │ ◀────────────┘
               ▼             │                ▼
          ┌──────────┐      │        ┌─────────────────┐
          │FETCH LINE│ 440  │        │ UPDATE DATA PER  │ 450
          └──────────┘      │        │ WRITE REQUEST    │
               │            │        └─────────────────┘
               ▼ ◀──────────┘                │
          ┌──────────────┐                   │
          │RETURN DATA TO │ 425               │
          │REQUESTING AGENT│                  │
          └──────────────┘                    │
               │ ◀─────────────────────────────
               ▼
          ┌─────────────────────┐
          │ ONCE REQUEST COMPLETED│ 430
          │ REMOVE FROM REQUEST   │
          │ BUFFER                │
          └─────────────────────┘
               │
               ▼
            ◇ MORE
            PENDING REQUESTS IN   Y
            BUFFER?          ──────────┐
              435                      │
               │ N
               ▼
          ┌─────────┐
          │   END   │
          └─────────┘
```

FIG. 4

"A METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS TO
COHERENT MEMORY IN A DISTRIBUTED MEMORY, CACHE COHERENT, MULTI-PROCESSOR SYSTEM"
by Manoj Khare, Akhilesh Kumar, Lily P. Looi
Docket No. P9301   Contact: Cynthia Thomas Faatz   Reg. No. 39,973   Phone No. 53-268-1442
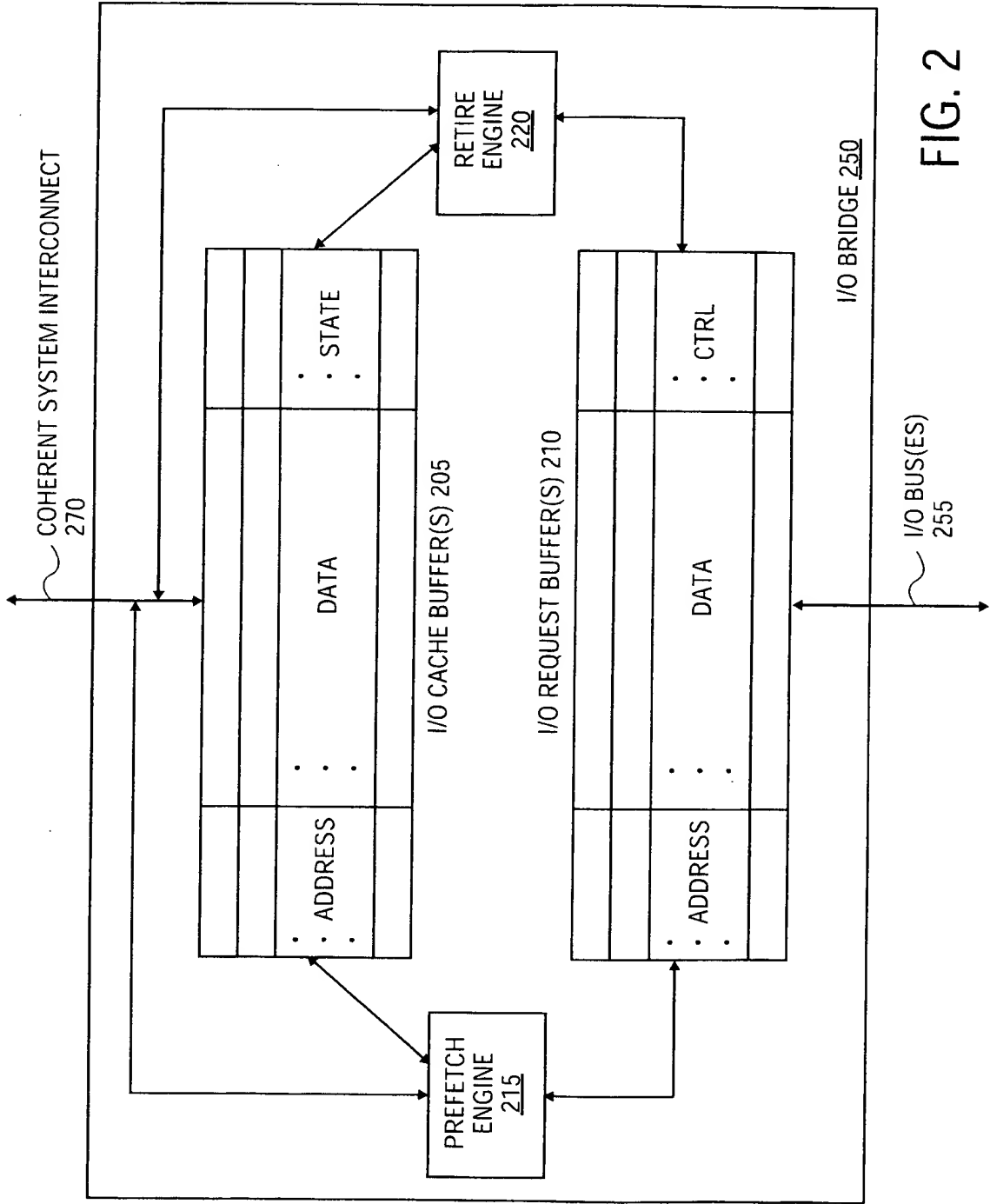Sheet 5 of 5
REPLACEMENT SHEET

```
                        ┌─────────┐
                        │  BEGIN  │
                        └────┬────┘
                             │
                             ▼
              ┌──────────────────────────────┐
              │    BUFFER I/O TRANSACTIONS    │
              │    DIRECTED TO A DISTRIBUTED  │
              │    COHERENT MEMORY FROM AN    │
              │           I/O BUS             │
              └──────────────┬───────────────┘
                             │
                             ▼
              ┌──────────────────────────────┐
              │   PREFETCH DATA FROM MEMORY   │
              │  IN RESPONSE TO FIRST BUFFERED│
              │        I/O TRANSACTION        │
              └──────────────┬───────────────┘
                             │
                             ▼
              ┌──────────────────────────────┐
              │  TEMPORARILY STORE PREFETCHED │
              │             DATA              │
              └──────────────┬───────────────┘
                             │
                             ▼
              ┌──────────────────────────────┐
              │  MAINTAIN COHERENCY BETWEEN   │
              │  PREFETCHED DATA AND DATA     │
              │  STORED IN COHERENT MEMORY    │
              └──────────────┬───────────────┘
                             │
                             ▼
              ┌──────────────────────────────┐
              │      RETIRE BUFFERED I/O      │
              │     TRANSACTIONS IN ORDER     │
              └──────────────┬───────────────┘
                             │
                             ▼
                        ┌─────────┐
                        │   END   │
                        └─────────┘
```
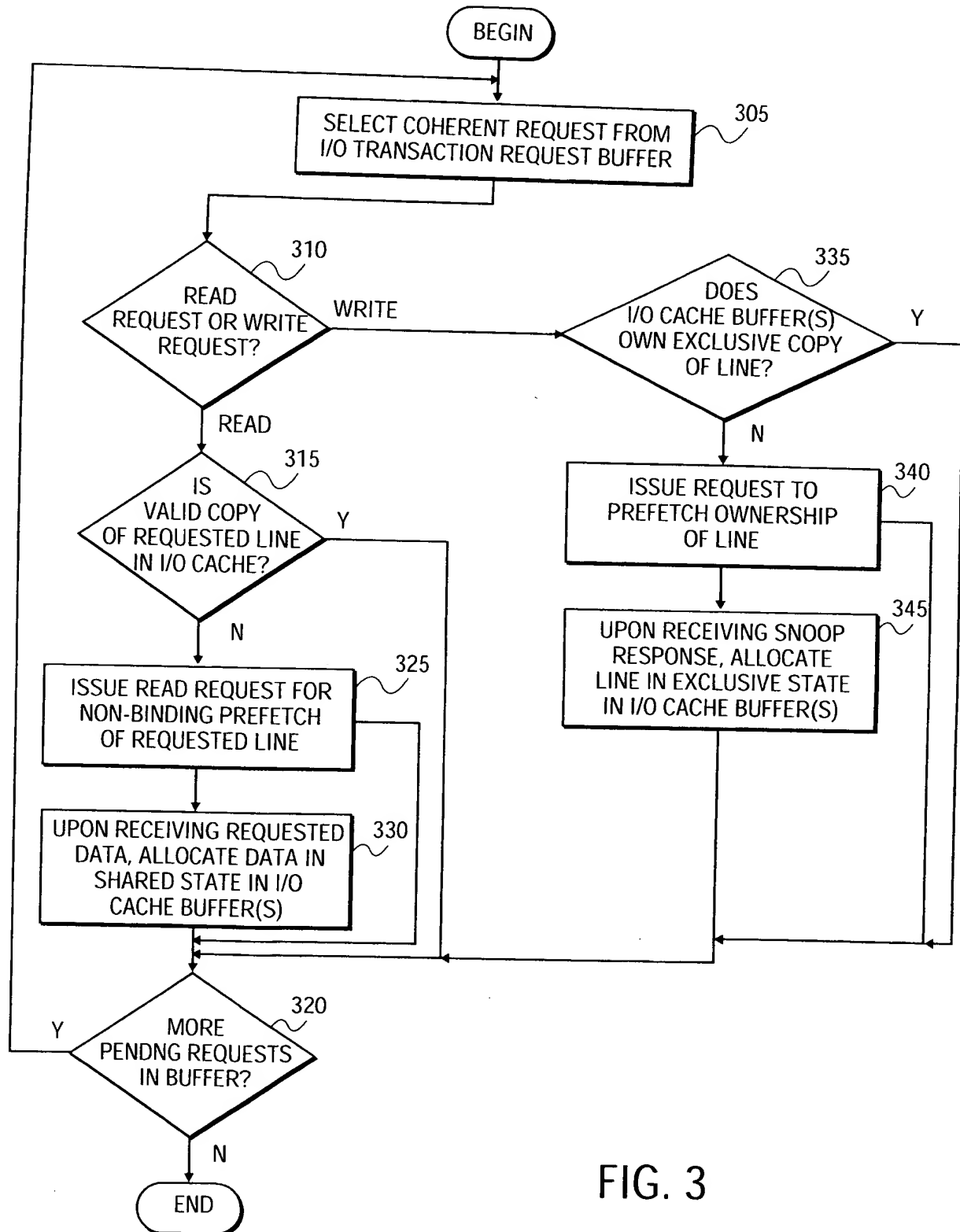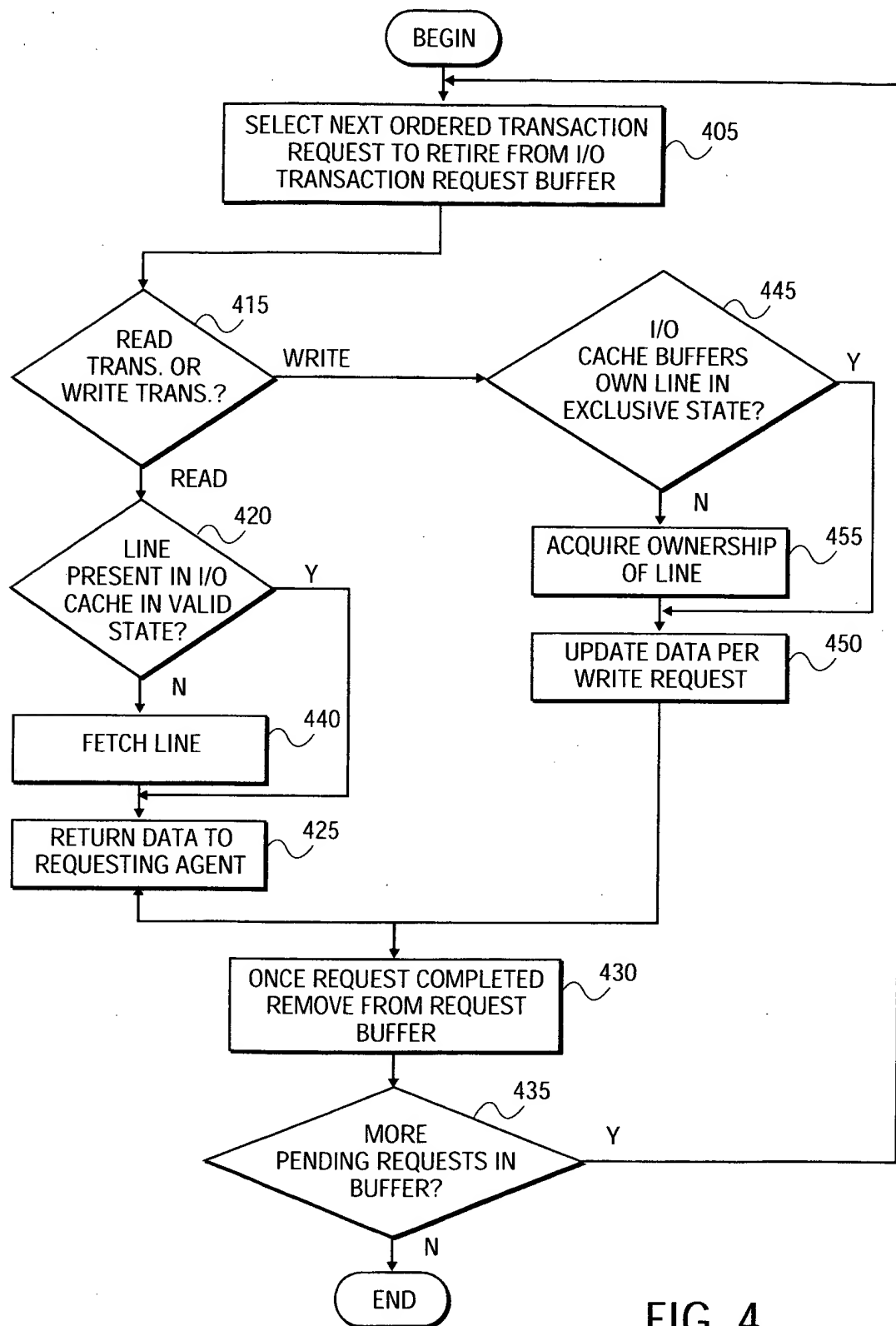
FIG. 5